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FUJITSU

DATA SHEET

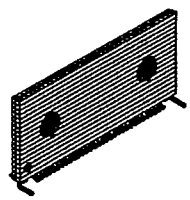
MB814953
4.5 MBIT RDRAM™

ADVANCED INFORMATION

DESCRIPTION

The MB814953 is a new generation ultra high speed CMOS Rambus™ DRAM organized as 512KX9. The MB814953 uses advanced circuit design techniques with standard CMOS process technology. It utilizes the 18,432 sense amplifiers as a cache and bursts up to 256 bytes at a rate of 500 MBytes per second. The device is an ideal choice for main memory and graphics applications where high–performance and low cost are required.

MB814953–P



PLASTIC VSMP
(VSMP-32P-M01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- Rambus Interface:
  500 MB/sec peak transfer rate per RDRAM
  Low signal swing byte wide (9 bits) interface to the Rambus Channel
  Synchronous protocol for fast block–oriented data transfers
  Flexible addressing controlled by on–chip registers
  Direct connection to Rambus ASICs, MPUs, and Peripherals
- 48 ns from beginning of read request to first byte, 2 ns per byte thereafter
- 2 cache lines per RDRAM – Each cache line is 1 KByte each (9–bit bytes)
- RDRAM entirely self–contained
- Vertical surface mount package

SYSTEM BENEFITS

- Same pinout for 18 Mbit RDRAM
- Incremental memory granularity is 512KB
- Alleviates need for expensive multi chip modules at high system clock rates
- Systems are modular – faster MPUs and larger Rambus memories can be installed without changing board layout or logic design

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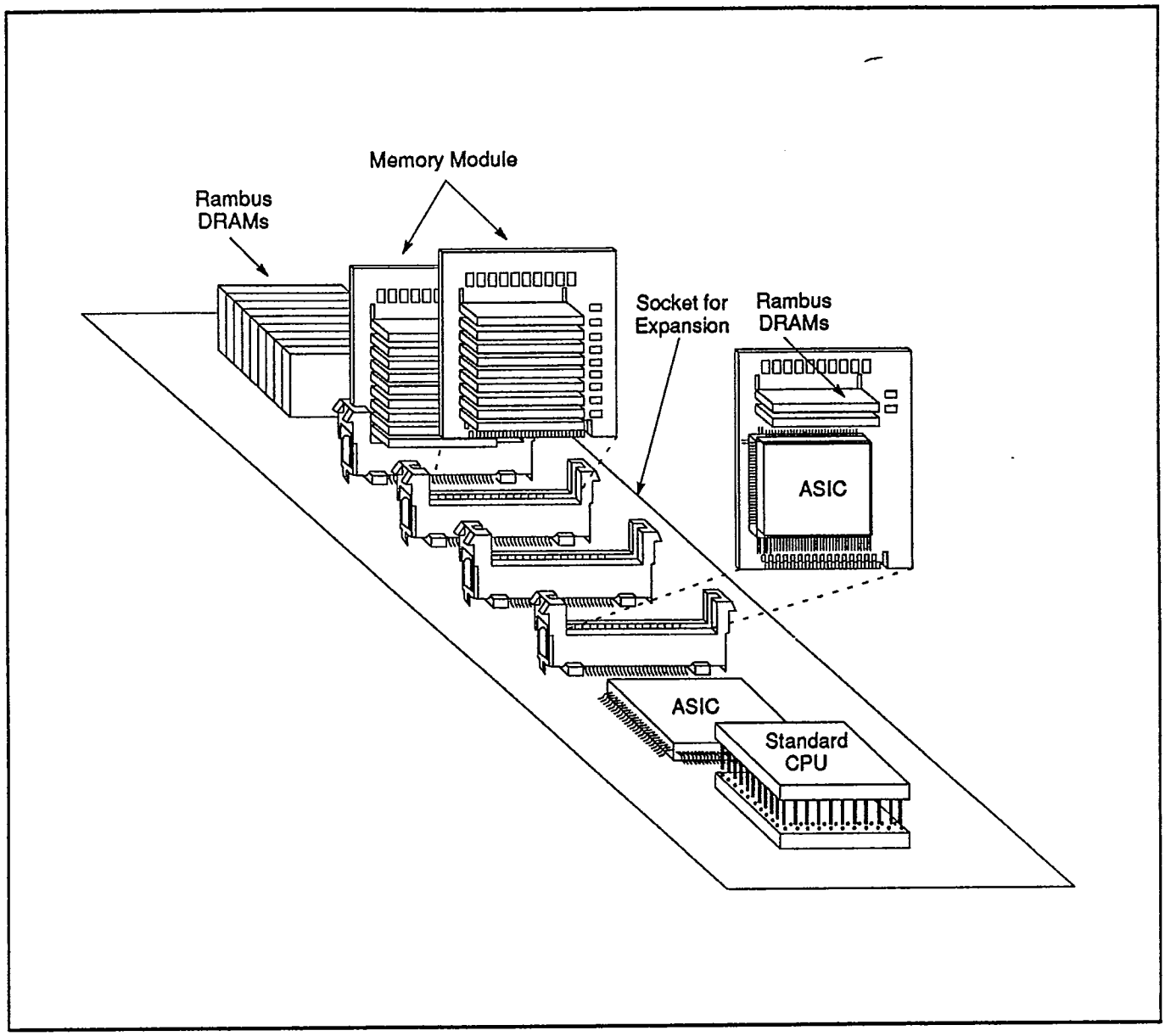
SYSTEM CONFIGURATION



The MB814953 contains a DRAM core, DRAM controller, and Rambus™ Interface Circuitry. The Rambus Interface circuitry and DRAM control logic manage access to the DRAM core.

PROTOCOL

The MB814953 responds to bus transactions initiated by a Rambus master device. The Rambus master sends out a request packet on the Rambus Channel and all RDRAM devices on the bus receive the information in the request packet. The request packet contains address and control information necessary to specify the transaction. The transaction can be a read or a write operation from or to a block of memory between 1 and 256 bytes in length.

The MB814953, like other RDRAMs on the Rambus Channel, examines the contents of each request packet to determine the required action. If the address in the packet targets this particular RDRAM, then the RDRAM replies with an Acknowledge packet which indicates to the master whether the RDRAM can service the request. For memory write transactions, the master follows the request packet with the write data packet, which is stored by the MB814953 into the DRAM core's column sense amplifiers. For memory read transactions, the RDRAM reads data from the DRAM core's sense amplifiers and sends it to the master. The interval between the request packet and the following acknowledge and data packets is programmable during device initialization. Once programmed, the delays are fixed during normal operation.

CACHING

The MB814953 contains two completely independent direct mapped cache banks. Each bank has its own DRAM sub–array, sense amplifiers, and cache tag. The Rambus Interface circuitry manages both the DRAM core and cache operation. The master only needs to retry those transactions that caused a miss.

Each cache in the MB814953 is 1 KByte. The 1 KByte cache size contributes to a significant hit rate to these caches and the access time to data in these caches is very low.

If the data specified by the request packet is not available in the sense amplifiers, the RDRAM begins a DRAM row access operation to write back the current row and retrieve the requested row. Simultaneously, the MB814953 sends a Negative Acknowledgment packet to the requesting master device. The master may then retry the operation a few wait cycles later. The time before retry is the row miss parameter. The most recently requested rows are latched in the sense amplifiers until the master requests a new row. The sense amplifiers thus act as a cache for very fast read and write accesses.

ADDRESSING

Unlike standard DRAMs, each MB814953 decodes its own addresses. The mapping of addresses to Rambus devices is set during device initialization. The address mapping is very flexible, supporting device interleaving and mixing of Rambus devices of various sizes and types.

Address mapping, self–refresh, packet interval timing, and other functions are controlled by use of on–chip registers. Registers are accessed using the same read and write transactions as memory, but are located in separate address spaces.

PINOUT

32 pin VSMP
(TOP VIEW)

1	V_{DD}
2	Gnd
3	BusData8
4	Gnd
5	BusData7
6	(NC)
7	BusEnable
8	V_{DD}
9	BusData6
10	Gnd
11	BusData5
12	$V_{DD}A$
13	RClk
14	GndA
15	TClk
16	V_{DD}
17	BusData4
18	Gnd
19	BusCtrl
20	SIn
21	V_{REF}
22	SOut
23	BusData3
24	Gnd
25	BusData2
26	(NC)
27	BusData1
28	Gnd
29	BusData0
30	(NC)
31	Gnd
32	V_{DD}

PIN DESCRIPTION

Signal	I/O	Description
BusData [0 to 8]	I/O	Bus data for request, write, and read protocols These are low swing signals referenced to V_{REF} The data lines carry the request packet with the address, operation codes, as well as the count of the bytes to be transferred. Active low
RClk	I	Receive clock. This clock is aligned with incoming request and write data packets. This clock is completely synchronized with the request and data sent out on the Rambus™ Interface
TClk	I	Transmit clock: This clock is aligned with the data being sent out on reads as well as the acknowledge packets. This is a low swing signal referenced to V_{REF}
V_{REF}	I	This is the logic threshold voltage for low swing signals
BusCtrl	I	Control signals to frame packets, Transmit opcode, and acknowledge requests. Signal is active low
BusEnable	I	Control signals to enable the bus. this signal is pulsed to power up the bus. Long assertions of this signal will reset all devices on the bus. Signal is active low
V_{DD}, $V_{DD}A$		+5 V power supply. $V_{DD}A$ is a separate supply for clock receivers
Gnd, GndA		Circuit ground. GndA is a separate ground for clock receivers
SIn	I	Reset daisy chain input. CMOS levels. Active high
SOut	O	Reset daisy chain output. CMOS levels. Active high

RECOMMENDED DC OPERATING CONDITIONS (PRELIMINARY)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	4.75	5.25	V
$V_{IL, TTL}$	TTL input low voltage	−1.0	0.8	V
$V_{IH, TTL}$	TTL input high voltage	2.0	V_{DD} + 1.0	V
$V_{OL, TTL}$	TTL output low voltage	0	0.4	V
$V_{OH, TTL}$	TTL output high voltage	2.4	V_{DD}	V
V_{REF}	Reference voltage	1.7	2.4	V
V_{IH}	Input high voltage	V_{REF} + 0.2		V
V_{IL}	Input low voltage		V_{REF} − 0.2	V
V_{OH}	Output high voltage	V_{REF} + 0.3		V
V_{OL}	Output low voltage		V_{REF} − 0.3	V
I_{OL}	Output low current	−40	−10	mA
I_{OH}	Output high current	−10	10	µA
V_{TERM}	Termination voltage	2.2	2.7	V

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY)

Symbol	Parameter	Min	Max	Unit
RClk	Receive Clock Frequency	100	250	MHz
TClk	Transmit Clock Frequency	100	250	MHz

Figure 1. Read Hit Timing Diagram

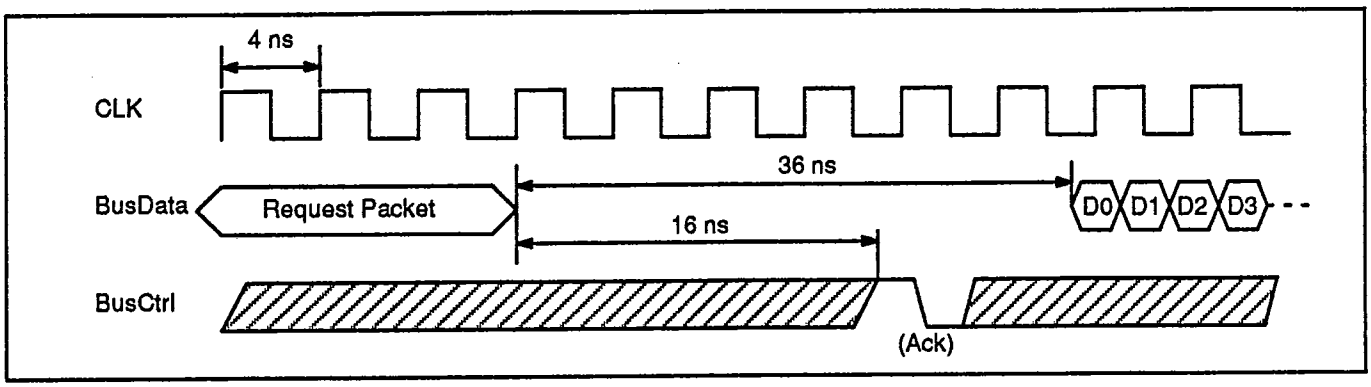


Figure 2. Write Hit Timing Diagram

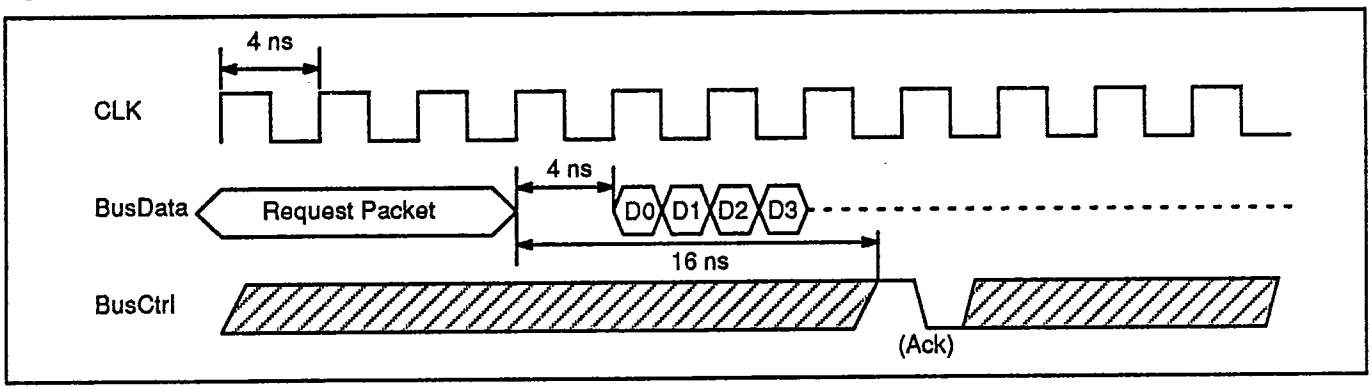


Figure 3. Read Miss Timing Diagram

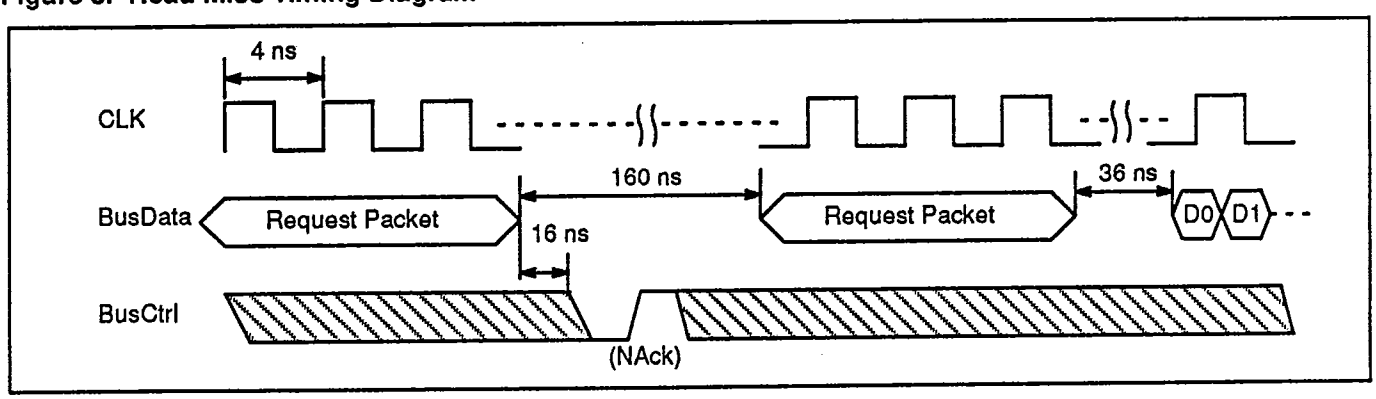
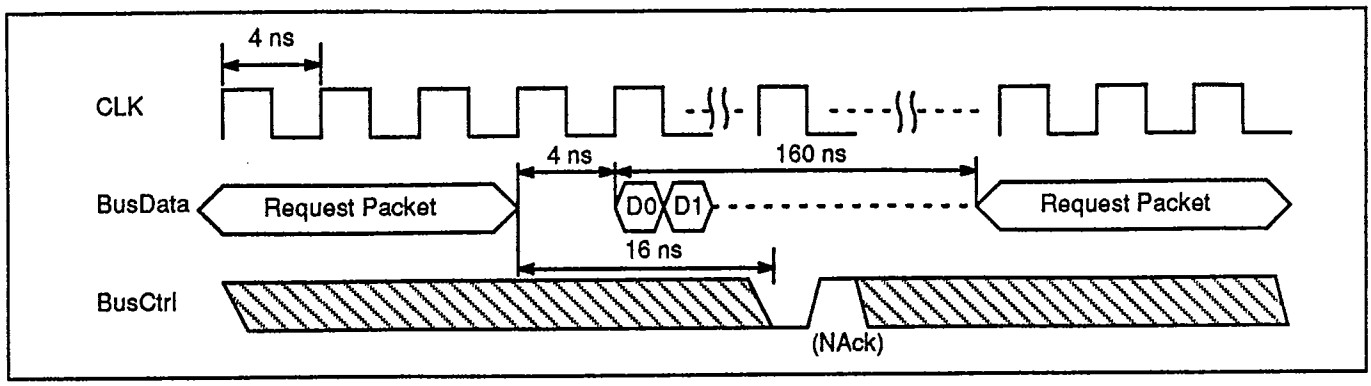
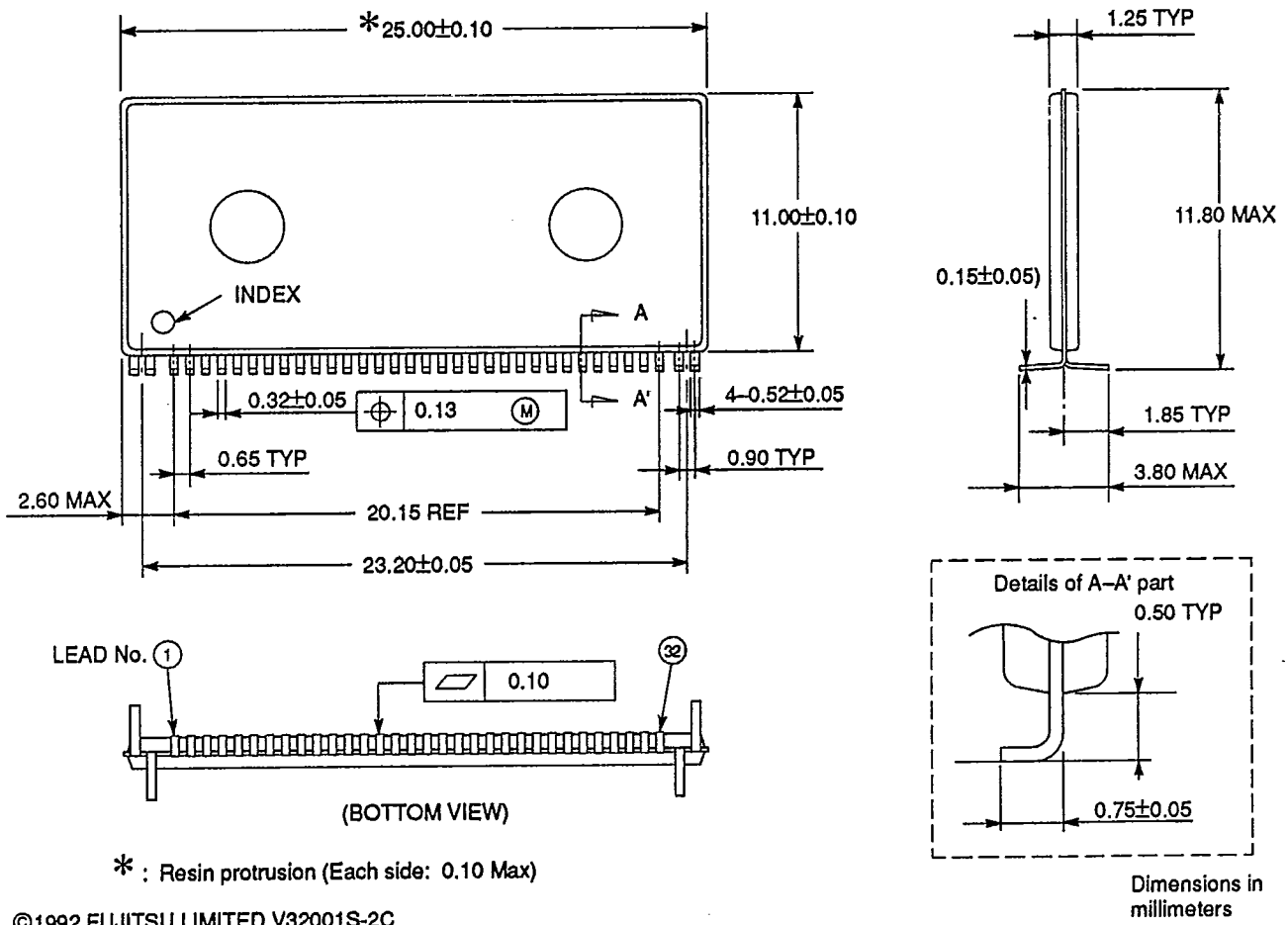


Figure 4. Write Miss Timing Diagram



PACKAGE DIMENSIONS

32-LEAD PLASTIC VERTICAL SURFACE MOUNT PACKAGE
(CASE No.: VSMP-32P-M01)



* : Resin protrusion (Each side: 0.10 Max)

Dimensions in millimeters